STRAS SPACE

PQ60
Interface Control Document

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List of Abbreviations

#-Q	Multiple of PocketQube standard height
COTS	Commercial Off the Shelf
GPIO	General Purpose Input/Output
NC	No Connect
PCB	Printed Circuit Board
PQ	PocketQube
S/C	Spacecraft
TBC	To Be Confirmed
TBD	To Be Determined
TT&C	Telemetry, Tracking, and Command

Normative References

[N1] PocketQube Standard, http://pocketqub.org/standard/

[N2] RFC 2119 – Key Words for Use in RFCs to Indicate Requirement Levels, S. Bradner, https://www.ietf.org/rfc/rfc2119.txt

[N3] High-speed (3.125 Gbps) Stacking Connectors, FX8C Series, http://www.hirose.co.jp/cataloge_hp/e57805019.pdf

[N4] I2C Bus Specification and User Manual, NXP document UM10204 rev 5, http://www.nxp.com/documents/user_manual/UM10204.pdf

[N5] Universal Serial Bus Specification, revision 1.1, September 1998.

[N6] Generic Standard on Printed Board Design, ANSI/IPC-2221, February 1998.

Supplementary References

[S1] DIYSats forum - “PocketQube Standard for COTS Boards”, http://diysats.com/viewtopic.php?id=8

[S2] StackableUSB Specification, version 0.77.A, June 2008, http://www.stackableusb.org/spec/StackableUSB_Specification.pdf

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Acknowledgements

The author would like to acknowledge the contributions of Stuart McAndrew, Tom Walkinshaw, Conor Forde, and the other members of the DIYSat forum, without whose input this work would not have been possible[1]. Any errors and misunderstandings are our fault.

1 If we've forgotten anyone who participated in the discussions, please let us know. It's not intentional!

0. Scope and rationale

This document describes the interfaces (mechanical, electrical, and logical) for a standard avionics bus inteneded for use in PocketQube spacecraft [N1]. The intent of this standard is to make it possible for low-cost COTS modules to be designed and manufactured, and to be integrated with spacecraft-specific payload modules. By making the standard relatively flexible, but still independent of exact S/C configuration, it is hoped that COTS modules may be mass-produced and tested with little bespoke engineering, allowing for tight cost control.

The general design approach is to use the lowest level of technology which is compatible with requirements. Many PQ missions are extremely cost-constrained, and cannot afford advanced manufacturing technologies. This is reflected in the PocketQube mechanical interfaces, which require only three precision-machined parts. As such, the interfaces presented in this document are intended to require only modest PCB manufacturing capabilities, which match up well with currently available offerings from very-low-cost board shops. It should be noted, however, that this standard does not constrain users from using more advanced technologies, should a need for those exist: the intent is that it should be **possible** to build a PocketQube using mature technologies, not that it be **necessary** to do so.

It is, of course, possible to construct spacecraft or S/C components which do not fully conform to this standard, and we anticipate that mission-specific components may well be out of compliance. However, we believe that any components which are meant to be reused will see the widest possible deployment if they do conform fully; similarly, non-conforming sub-assemblies, which nonetheless are designed with the PQ60 interface in mind, should be able to be integrated with COTS unit.s

The standard is referred to as PQ60 as it is intended for PocketQubes, and utilizes a 60-contact connector.

In the remainder of this document, the phrases “shall”, “shall not”, “should”, “should not”, and “may” have meaning as defined in [N2].

1. Design overview

PCBs which conform to PQ60 are intended to be stacked using a pair of inter-PCB (“mezzanine-style”) connectors, as shown in Figure 1, below. This avionics stack may be oriented within the S/C structure in any convenient orientation – for a 1-Q spacecraft, this does not matter, while larger spacecraft may place the stack aligned with the S/C long axis, or perpendicular to it.

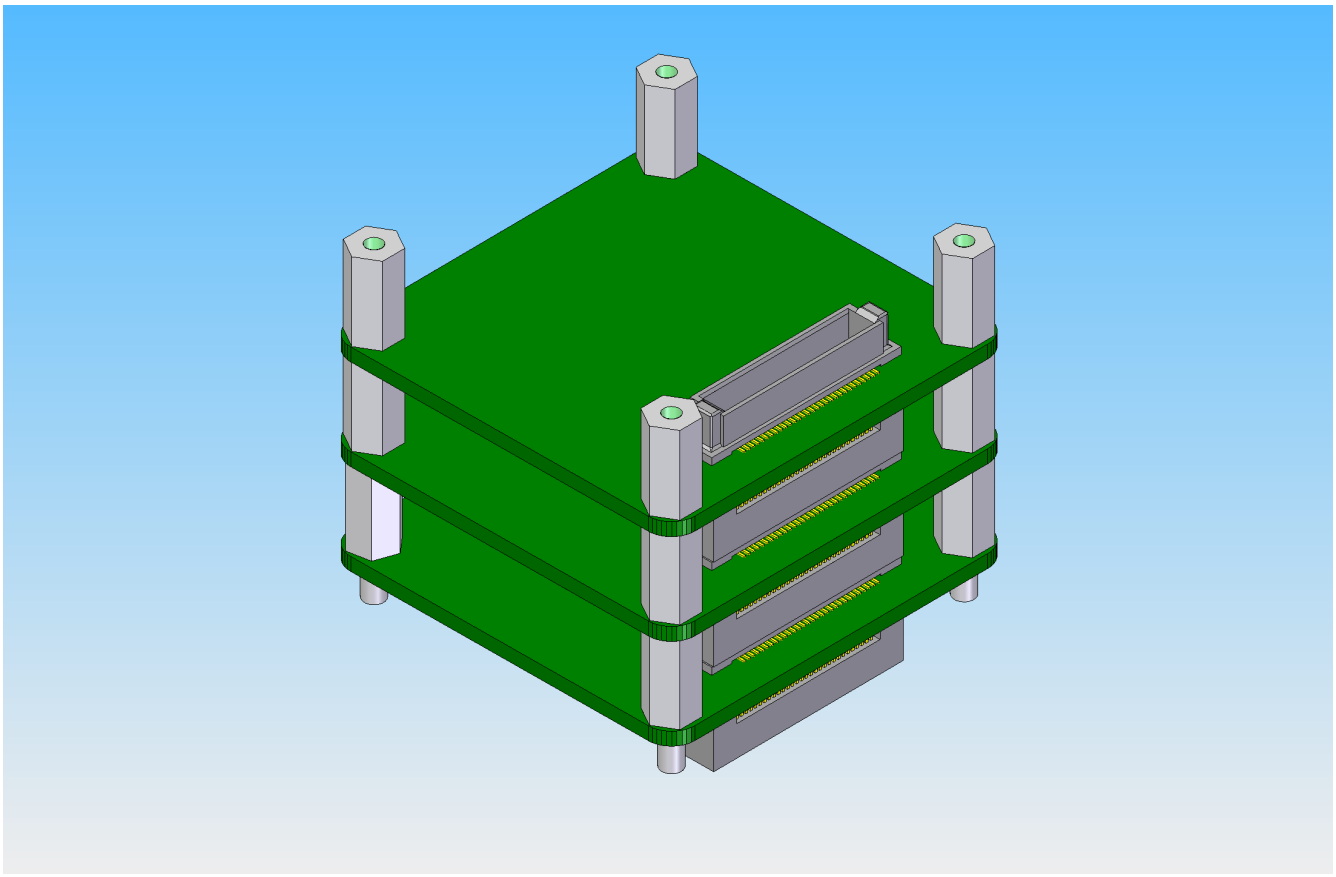

Figure 1: PQ-60 stack concept.

The overall layout of the spacecraft is not specified here, and so neither is the standard stacking order. It is expected that radios (which require access to externally-located antennas) will tend to be located towards one end of the stack, while power systems with their heavy batteries will be located in the middle. However, the interface is designed such that as few constraints as possible are placed on the S/C integrator.

For the purposes of this document, each PCB is defined as having a "top" and a "bottom" side. The distinction is somewhat arbitrary, as both sides of the PCB may be populated with parts. Conceptually, a stack would be assembled "bottom-up"; however, this is not a requirement specified by this document. Ultimately, the only distinction between "top" and "bottom" is the gender of the connector present on the PCB.

2. Mechanical interfaces

Each conforming PCB shall have a mechanical outline as shown in Figure 2 Four mounting holes are provided, each of which will clear an M2.5 or ANSI #4 screw. This allows for the use of threaded male-female standoffs or unthreaded female standoffs with threaded tie rods to assemble the stacks.

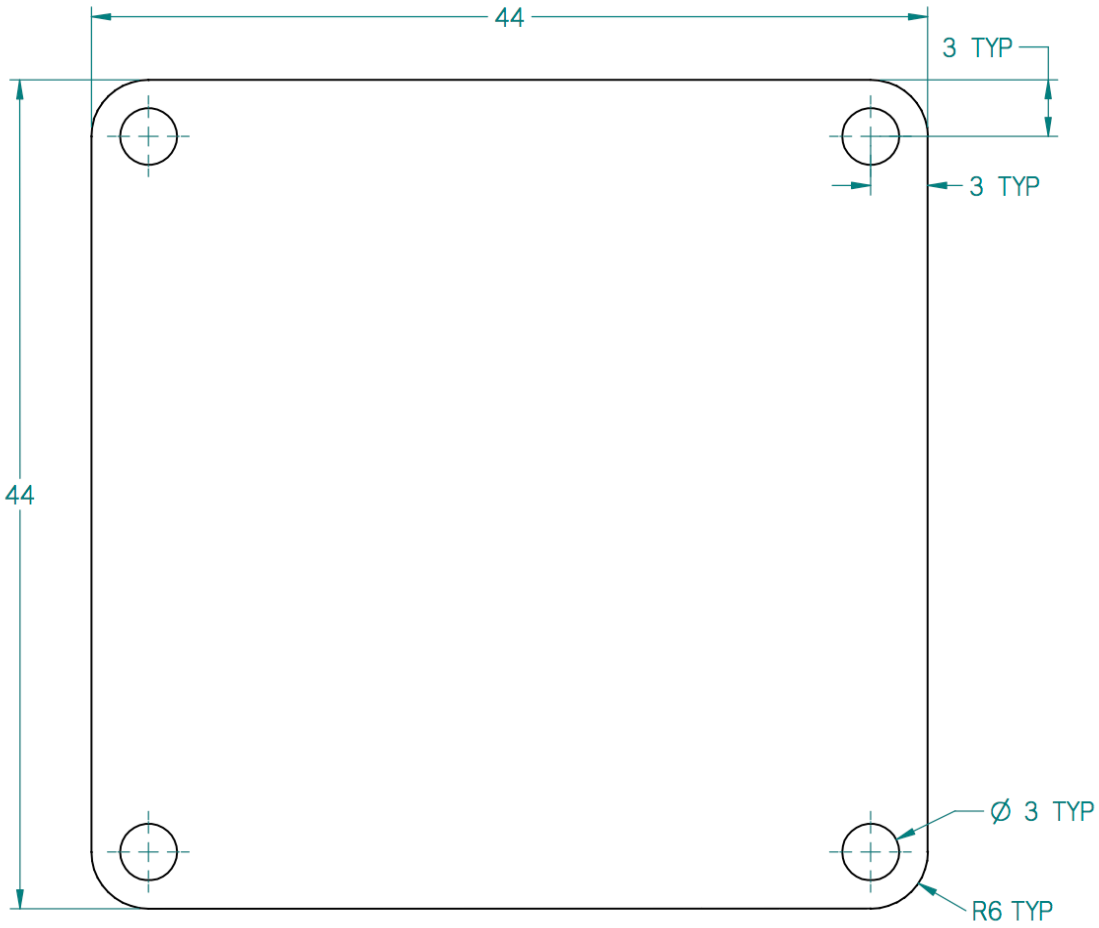

Figure 2: PQ-60 mechanical dimensions.

The primary thermal path for heat dissipation is through the mounting standoffs; it is expected that the PCB stack is thermally coupled to the structure. Given the low overall mass of a PocketQube, it is expected that the entire spacecraft is isothermal. A copper annulus of 6 mm diameter may be present around the mounting holes. If this annulus is present, it shall be DC isolated from PCB (and spacecraft) ground. The annulus should be connected to PCB ground via a 100 nF capacitor, for AC decoupling.

To allow for clearance of mounting hardware and components, Figure 3 describes the allowed envelope for parts, while Figure 4 describes keepout zones. Four keep-out areas have been defined for the mounting standoffs. The envelopes for parts are dependent on the exact connectors which are installed. On the bottom side, a standard height (S-SV) connector permits a 2 mm maximum part height, while a tall (S-SV5) connector permits a 7 mm maximum part height. On the top side, the maximum part height is as follows:

Connector	Maximum part height
P-SV	2 mm
P-SV1	3 mm
P-SV2	4 mm
P-SV4	6 mm
P-SV6	8 mm

Table 1: Top PCB side maximum component height.

A COTS unit shall document the height of connectors used, to allow the end user to budget available stack height.

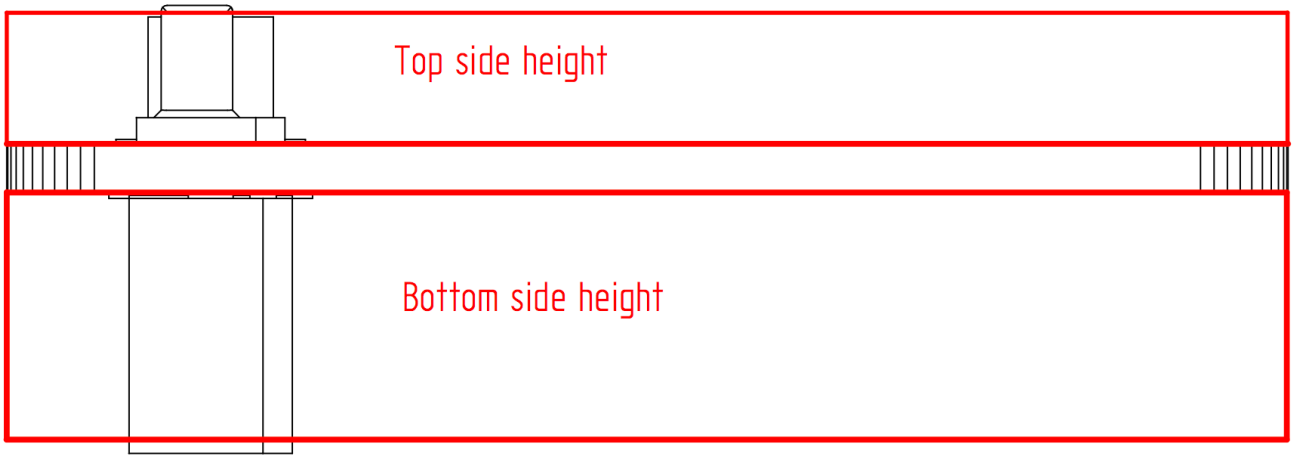

Figure 3: Parts placement envelope.

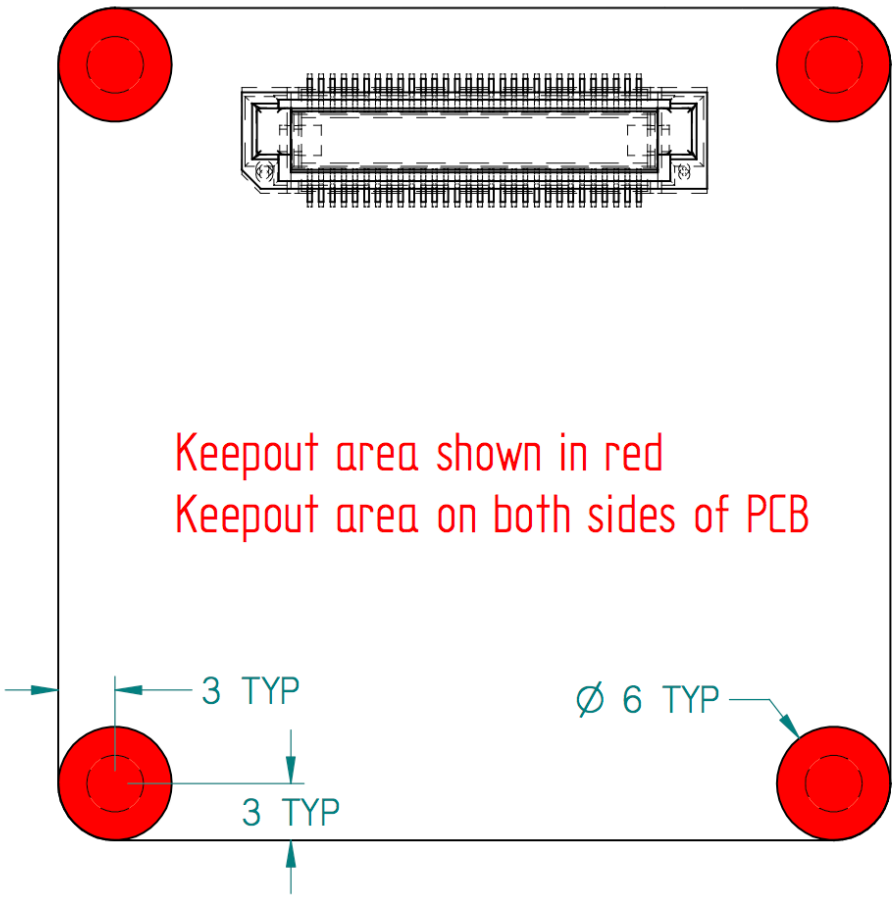

Figure 4: Keepout areas.

This combination always allows for a 1 mm gap between the top of one PCB and the bottom of the next PCB in a stack.

3. Electrical interfaces

3.1. Connectors

Figure 5 shows the location of the inter-PCB connectors. The PQ60 interfaces utilizes Hirose FX8C [N3] mezzanine connectors, with 60 contacts in a single row. The bottom side connectors are of the receptacle type; the part numbers are FX8C-60S-SV(92) for the standard height connector, and FX8C-60S-SV5(92) for the tall connector. Note that the number in parentheses is a connector packaging option, and may vary from supplier to supplier.

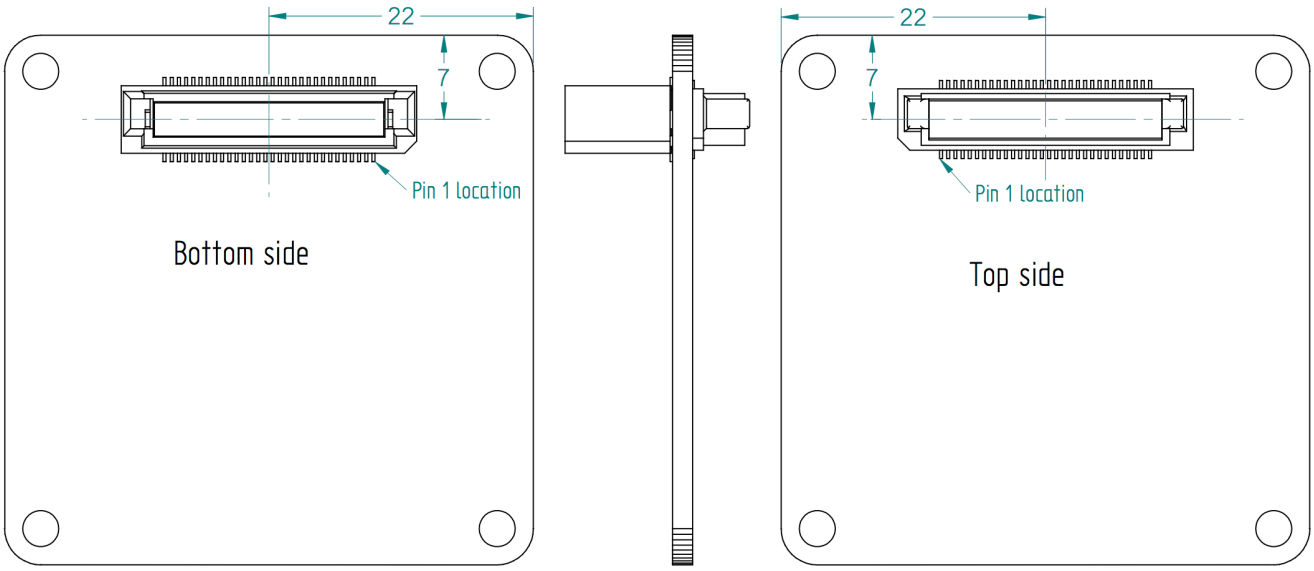

Figure 5: Connector locations.

The top side connectors are of the header type; the part numbers are FX8C-60P-SV(92), FX8C-60P-SV1(92), FX8C-60P-SV2(92), FX8C-60P-SV4(92), and FX8C-60P-SV6(92), depending on the required connector height. Again, the number in parentheses is a connector packaging option, and is likely to vary from supplier to supplier.

As Hirose does not define pinouts, Figure 5 also shows the connector pin numbering. This follows the standard numbering convention for dual inline packages used for semiconductors.

Table 2 shows the assignment of connector contacts to circuits. Each circuit is described elsewhere in this document. It is important to note that the circuit assignment is identical for both connectors on each PCB. Signals which are marked as "NC" shall be passed straight through the PCB, and shall not be connected to circuits on the PCB.

Contact	Function	Function	Contact
1	GND	USB_P	60
2	SCL	GND	59
3	GND	USB_N	58
4	SDA	GND	57
5	GND	NC	56
6	VBUS_SW1	VBUS	55
7	VBUS_SW2	VBUS	54
8	VBUS_SW3	VBUS	53
9	+3.3V_SW1	+3.3V	52
10	+3.3V_SW2	+3.3V	51
11	+3.3V_SW3	+3.3V	50
12	GND	GND	49
13	SCK	GND	48
14	GND	/SS	47
15	MISO	GND	46
16	GND	/RST	45
17	MOSI	GND	44
18	GND	NC	43
19	GPIO1	NC	42
20	GPIO2	GND	41
21	GPIO3	GPIO14	40
22	GND	GPIO13	39
23	GPIO4	GPIO12	38
24	GPIO5	GND	37
25	GPIO6	NC	36
26	GND	NC	35
27	GPIO7	NC	34
28	GPIO8	GND	33
29	GPIO9	GPIO11	32
30	GND	GPIO10	31

Table 2: Connector circuit assignments.

3.2. Signals

The various signals present on the PQ are grouped into several categories, as shown in Table 3. Each group is defined as being bus-global, or PCB-local, as shown in the table. The groupings are used to dictate how signals are broken out from connectors to the PCB electronics, and how they are passed from one PCB to another. The methodology used to do this is described elsewhere in this document.

With a few exceptions (noted below), most signals are optional, and may not be present in any given S/C configuration. However, PQ60 PCBs shall route all signals from the bottom to the top layer according to the guidelines specified for each signal.

Group	Type	Signals
Unswitched power	Bus-global	VBUS, +3.3V, GND
Switched power	PCB-local	VBUS_SW1 – VBUS_SW3, +3.3V_SW1 - +3.3V_SW3
Communications	Bus-global	SCL, SDA, USB_P, USB_M, SCK, /SS, MISO, MOSI, /RST
GPIO	PCB-local	GPIO1 – GPIO14

Table 3: Signal groupings.

3.2.1. GND

The GND signals represent the S/C global electrical ground. All GND signals on the connector shall be connected together in at least one point on the S/C (typically at the power system). All signals on the connector are referred to the GND net. When passing the GND circuit from one side of the PCB to the other, vias and traces shall be sized for a total current of 3 A.

This signal is mandatory.

3.2.2. VBUS

The VBUS signal represents the “raw” S/C bus voltage. This is typically the solar array or battery voltage, depending on the architecture of the power system. All VBUS nets shall be tied together in at least one point (typically at the power system). The VBUS signal shall be between 3.3 V and 5.5 V DC whenever the S/C is under power (*i.e.*, has power available; this specification does not apply to, for instance, batteryless S/C during eclipse). The power system should assert the /RST signal whenever VBUS drops below 3.3 V.

The VBUS signal is unswitched; PCBs which use it should take care to protect the rest of the S/C during fault conditions.

When passing the VBUS circuit from one side of the PCB to the other, vias and traces shall be sized for a total current of 3 A.

This signal is mandatory.

3.2.3. +3.3V

The +3.3V signal represents a regulated, unswitched voltage of +3.3 V ± 5%. All +3.3V nets shall be tied together at at least one point (typically at the power system). The generator of this signal shall ensure that the voltage on the +3.3V net is always less than or equal to that on the VBUS net, to assist

in PCB power sequencing.

The +3.3V signal is unswitched; PCBs which use it should take to protect the rest of the S/C during fault conditions.

When passing the +3.3V circuit from one side of the PCB to the other, vias and traces shall be sized for a total current of 3 A.

This signal is mandatory. At a minimum, the power system (or other system) shall supply 25 mA on the +3.3V rail, as open-drain communications lines are pulled to this level. A higher supply current on this rail is optional.

3.2.4. VBUS_SW1 – VBUS_SW3

The three VBUS_SW*x* circuits carry a switch-controlled bus voltage. The voltage levels present are identical to VBUS (+3.3 V to +5.5 V DC); however, each individual circuit is switched by the power system.

The power system should protect these circuits from overcurrent; any PCBs which use these circuits should also take care to protect the power system from fault conditions.

When passing the VBUS_SW*x* circuits from one side of the PCB to the other, vias and traces shall be sized for a current of 1 A per circuit.

These signals are optional. If they are not present, the missing signals should be tied to GND in at least one point in the S/C.

3.2.5. +3.3V_SW1 - +3.3V_SW3

The three +3.3V_Sw*x* circuits carry a switch-controlled +3.3 V ± 5% voltage. Each circuit is individually switched by the power system.

The power system should protect these circuits from overcurrent; any PCBs which use these circuits should also take care to protect the power system from fault conditions.

When passing the +3.3V_SW*x* circuits from one side of the PCB to the other, vias and traces shall be sized for a current of 1 A per circuit.

These signals are optional. If they are not present, the missing signals should be tied to GND in at least one point in the S/C.

3.2.6. SCL and SDA

These circuits carry the primary bus communications channel, and correspond to the clock (SCL) and data (SDA) lines of a 100 kb/s I^2C channel [N4].

Cards shall load these circuits with no more than 10 pF of parasitic capacitance. When passing these circuits from one side of the PCB to the other, good high-frequency practices should be followed.

Both circuits shall be pulled up to the +3.3V (unswitched) circuit in at least one point on the spacecraft; multiple pull-ups may be present. The total pull-up resistance shall be smaller than 5 kΩ (for a single-point pull-up). If multiple pull-up resistors are present, the total pull-up resistance shall be greater than 1.1 kΩ.

The logic levels for the I^2C bus shall be $V_{IL,max}$ of 1.0 V, and $V_{IH,min}$ of 2.3 V, consistent with [N4] and a pull-up voltage of 3.3 V. Drivers shall be capable of driving low to a $V_{OL,max}$ of 0.4 V when sinking 3 mA.

The standard I^2C timeout (28 ms of SCL low) should be implemented, with all devices connected to I^2C resetting their communications controllers when this timeout expires.

These signals are mandatory.

3.2.7. USB_P and USB_M

These circuits carry a single USB 1.1 [N5] channel. The USB_P circuit corresponds to the D+ signal, and USB_M corresponds to the D- signal of the USB specification. No function is currently assigned to these circuits.

When passing these circuits from one side of the PCB to the other, good high-frequency practices should be followed. If a card connects to these circuits, the loading on the net shall be kept within the limits specified by [N5].

These signals are optional. If they are present and in use, VBUS shall be a regulated 5 V ± 5% bus, as specified in [N5]. The USB_P and USB_N lines shall be pulled to VBUS and GND as required in [N5]. If they are not present, they should be connected to GND via 100 kΩ.

3.2.8. SCK, /SS, MISO, and MOSI

These circuits form a single SPI channel, which is intended for connection to the TT&C subsystem. The signal assignments are as follows:

Signal	Function
SCK	Clock
/SS	Slave select
MISO	Master in, slave out
MOSI	Master out, slave in

The signals shall be push-pull, with a $V_{OL,max}$ of 0.6 V and a $V_{OH,min}$ of 2.7 V when sinking/sourcing 2 mA of current, and a V_{IL} of 0.6 V and a V_{IH} of 2.7 V.

These signals are optional. If they are not present, an alternate scheme for communicating with the TT&C system must be present, and these circuits should be tied to GND via 100 kΩ.

3.2.9. /RST

This circuit represents an S/C-wide reset and load-shed signal. It is an active-low, open-drain signal which may be asserted by the power system, TT&C system, or any other system which has the authority to reset the spacecraft.

When asserted, this signal shall have a $V_{OL,max}$ of 0.5 V at a sink current of 1 mA. A pulse width of at least 100 ms shall be driven, and the reset signal shall be active low. This signal shall be pulled to VBUS via a 10 kΩ resistor at one point in the S/C.

This signal is optional. If it is not present, it shall be tied to VBUS via 10 kΩ.

3.2.10. GPIO1 – GPIO14

These circuits represent general purpose I/O signals for the S/C. No particular requirements are placed on these, as they are mission-specific.

When passing the GPIO*x* signals from one side of the PCB to the other, vias and traces shall be sized to carry a minimum of 100 mA of current. Traces shall be kept separated by at least 0.05 mm from other circuits; this allows for each circuit to carry a voltage of up to 30 V DC. For reference, this is class B4, as defined in [N6].

3.3. Connections

It is the intent of the PQ60 specification to allow users to "snap" together custom and COTS modules in order to assemble a spacecraft. In order to minimize costs of COTS modules, we have designed the interface in such a way that modules need no per-spacecraft customization before use. By doing this, modules can be mass-produced and mass-tested, and so can be delivered quickly and cheaply.

In order to allow for flexibility in S/C configuration, a "signal shifting" scheme is utilized on the PQ60 bus. This scheme is similar to that used by the StackableUSB standard [S2]. This scheme is detailed in this section.

In this scheme, bus-global signals are distributed uniformly through the bus stack: PCBs connect the circuits on the bottom side connector to the top side connecor. If a PCB requires a particular signal, it taps into it in a multi-drop configuration.

PCB-local signals are treated differently. Within each signal group, a PCB is permitted to use zero or more signals for its own exclusive purposes. Signals are considered to be fed into the PCB on the bottom side connector. Signals which are required by the PCB are routed from the bottom side connector into PCB circuitry. The signals which are used are the lowest-numbered signals within the group. Unused signals are routed from the bottom of the PCB to the top. However, rather than being routed straight through (as global signals are), they are routed to the lowest-numbered signals within the group, replacing the signals which were "consumed" by the PCB.

This is best demonstrated via examples. The examples below show the routing on a PCB which uses bus-global signals, a PCB which uses a single switched power rail, and a PCB which uses two switched power rails and three GPIO resources.

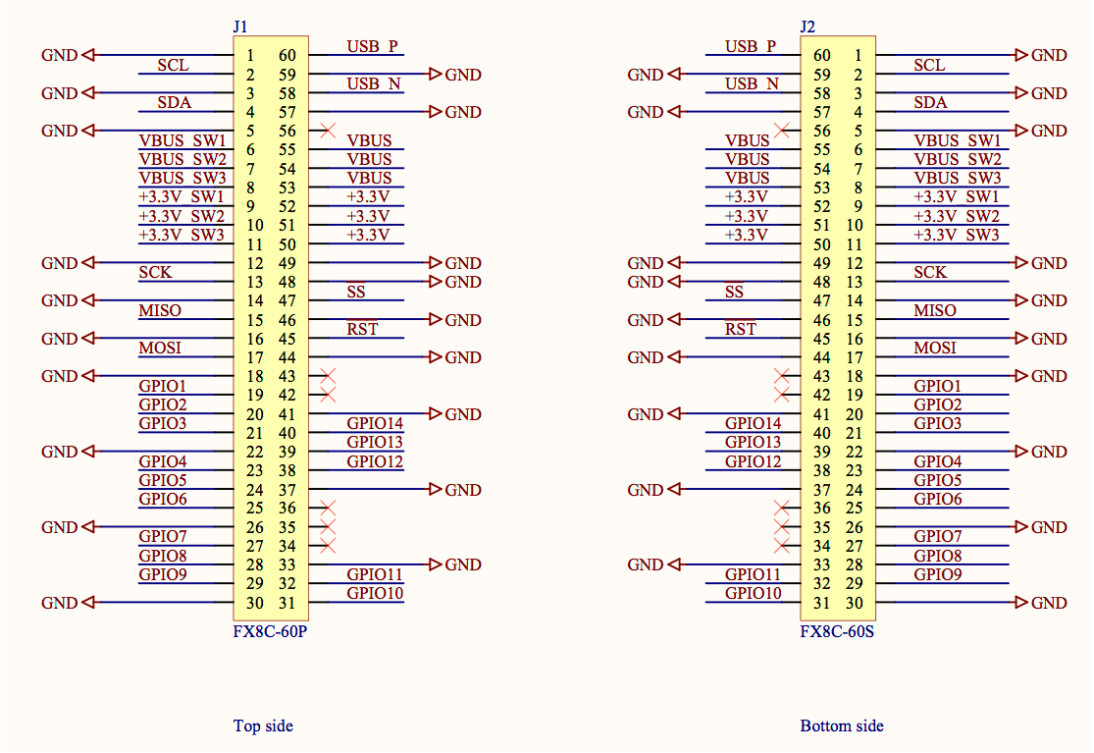

Figure 6: Passthrough connections on a PQ-60 PCB which does not consume any resources.

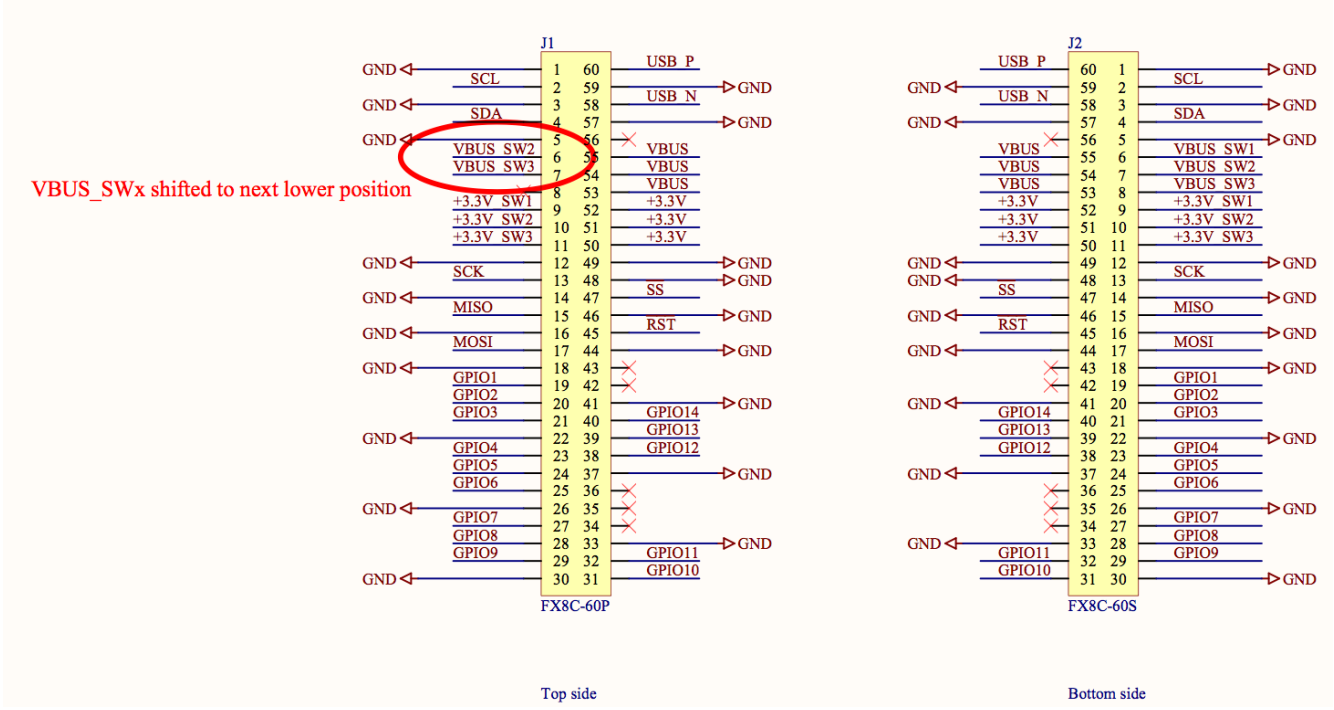

Figure 7: Passthrough connections on a PQ-60 PCB which consumes a single switched power rail.

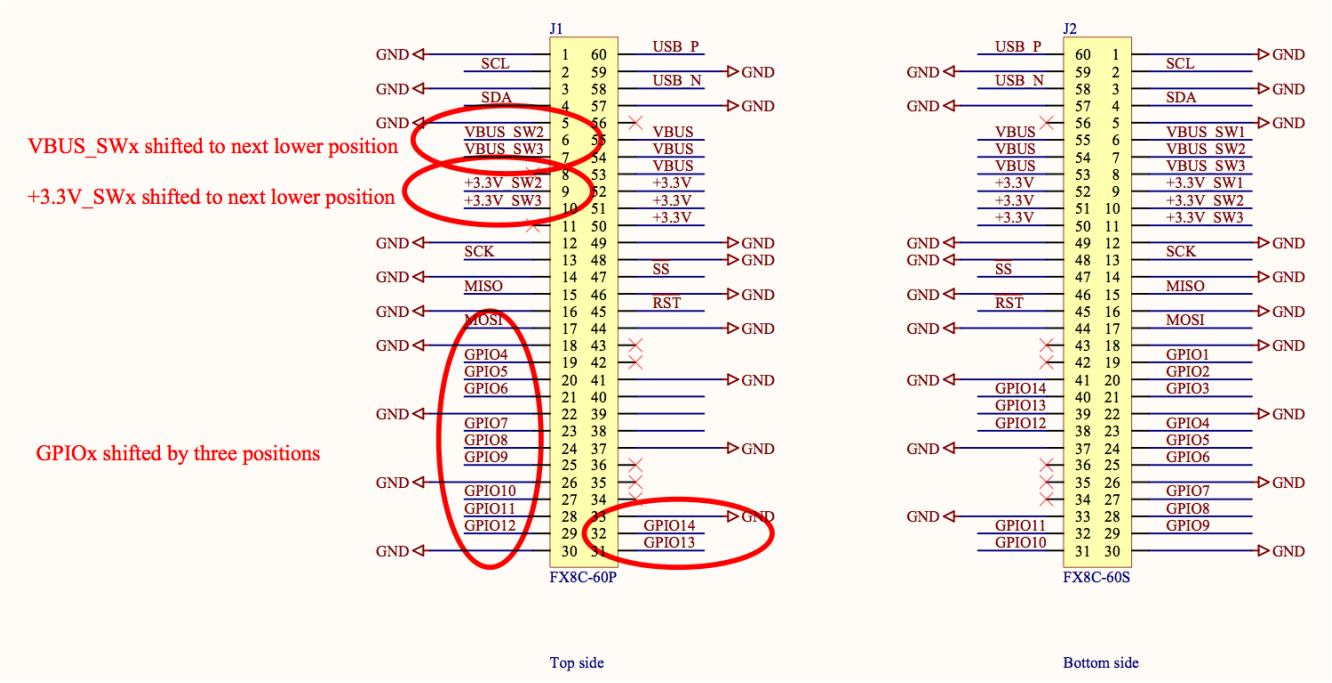

Figure 8: Passthrough connections on a PQ-60 PCB which conumes two power rails and three GPIOs.

It should be noted that other options are possible: for example, a PCB could "inject" signals into the stack by shifting signals to higher-numbered positions, or it could intercept global signals and replace them. This document does not constrain such configurations, so long as the overall input-output behaviour of a PCB conforms to this specificiation.

4. Logical interfaces

This document does not specify the logical or higher-level interfaces for the PQ60 bus. Although I^2C is used as a low-level protocol, no further details are defined. Address allocation is the responsibility of the spacecraft integrator, who should work with module providers to define PCB addresses. Similarly, higher-level protocols are not defined. So long as unique I^2C addresses are used, multiple protocols should be able to inter-operate on the bus.

Devices on the bus should respond to the I2C General Call hardware reset mechanism (a write to address 0x00, with a data byte of 0x06; refer to section 3.1.14 of [N4]).